CLAIMS

1. A method for fabricating a nonvolatile memory, the method comprising:

(1) forming a first conductive gate for a nonvolatile memory cell;

(2) after the operation (1), forming conductive floating gates FG1 and FG2 for the memory cell.

2. The method of Claim 1 wherein the operation (2) further comprises forming conductive gates CG1 and CG2 for the memory cell, wherein the gates CG1, CG2 are insulated from each other and from the first conductive gate.

3. The method of Claim 2 wherein the gate CG1 overlies the gate FG1, and the gate CG2 overlies the gate FG2.

4. The method of Claim 1 wherein the first conductive gate and the gates FG1 and FG2 overlie a semiconductor substrate and are insulated from the substrate;

wherein the memory cell comprises two source/drain regions in the substrate and a channel region extending between the two source/drain regions under the gates FG1 and FG2 and the first conductive gate.

5. The method of Claim 1 wherein a width of the fist conductive gate is smaller than the minimum photolithographic line width.

6. The method of Claim 1 wherein a width of the fist conductive gate is smaller than the width of any one of gates FG1, FG2.

7. The method of Claim 1 wherein forming the first conductive gate comprises:

forming a conductive layer; and

etching the conductive layer;

wherein the etching operation comprises horizontal etching to reduce the width of the first conductive gate.

8. The method of Claim 1 wherein forming the first conductive gate comprises:

forming a conductive layer;

etching the conductive layer to form a conductive feature having sidewalls;

reacting the material of the sidewalls with another material to form a reaction product on the sidewalls; and

removing the reaction product.

9. The method of Claim 8 wherein the reacting operation comprises oxidation of the material of the conductive layer to form an oxide on the sidewalls.

10. The method of Claim 8 further comprising, after removing the reaction product on the sidewalls, oxidizing the sidewalls to form a dielectric on the sidewalls to insulate the first conductive gate from the gates FG1 and FG2.

11. The method of Claim 1 wherein the nonvolatile memory cell is part of an array of nonvolatile memory cells, each memory cell of the array having conductive floating gates FG1 and FG2 and a first conductive gate;

wherein the method comprises, before the operation (1), performing the following operation:

(a) forming one or more substrate isolation regions in a semiconductor substrate between active areas of the semiconductor substrate, each substrate isolation region being a dielectric region protruding above the semiconductor substrate;

wherein the operation (1) comprises:

(b) forming one or more conductive lines G1, each conductive line G1 overlying at least one active area, wherein each first conductive gate comprises a portion of a line G1;

wherein the operation (2) comprises:

(c) forming a layer ("FG layer") over the first conductive lines and the substrate isolation regions, wherein each of the floating gates FG1, FG2 of each memory cell comprises a portion of the FG layer;

(d) partially removing the FG layer to expose the substrate isolation regions and to remove the FG layer from over at least a portion of each conductive line G1.

12. The method of Claim 11 wherein the operation (d) is terminated with reference to a time of detecting that the substrate isolation regions have been exposed.

13. The method of Claim 12 wherein each substrate isolation region traverses the memory array, and each conductive line G1 crosses over plural substrate isolation regions.

14. The method of Claim 11 wherein the top surface of each line G1 is planar but the bottom surface of each line G1 goes up and down over the substrate isolation regions.

15. The method of Claim 11 further comprising, before forming the FG layer, forming a dielectric over sidewalls of each conductive line G1 to insulate the conductive lines G1 from the floating gates.

16. The method of Claim 15 wherein each memory cell further comprises two second conductive gates insulated from the first conductive gate and the floating gates FG1 and FG2, and the method further comprises:

(e) after the operation (d), forming a dielectric D1 over the FG layer;

(f) forming a layer G2 over the dielectric D1, wherein each second conductive gate comprises a portion of the layer G2;

(g) partially removing the layer G2 and the FG layer to form the floating gates and to form from the layer G2 one or more conductive lines for the second conductive gates, wherein each second conductive gate comprises a portion of a conductive line formed from the layer G2.

17. The method of Claim 16 wherein in the operation (f), the layer G2 is formed to have a portion P1 protruding above each conductive line G1; and

the operation (g) comprises:

(g1) forming a layer L1 over the layer G2 such that the protruding portions P1 of the layer G2 are exposed and not completely covered by the layer L1;

(g2) at least partially removing the protruding portions P1 of the layer G2 to form a gap in the layer G2 over each line G1, wherein at a conclusion of this removing operation a portion of the layer G2 remains covered by the layer L1;

(g3) forming a layer L2 on the layer G2 adjacent to the gaps; and

(g4) removing at least parts of the layers L1 and G2 selectively to the layer L2.

18. The method of Claim 17 wherein the operation (g1) comprises:

forming the layer L1 over the entire layer G2; and

planarizing the layer L1 to expose the protruding portions P1.

19. The method of Claim 17 wherein the operation (g3) comprises reacting the layer G2 with another material to form the layer L2.

20. The method of Claim 19 wherein the reacting operation comprises oxidation of the layer G2.

21. The method of Claim 19 wherein the reacting operation comprises a chemical reaction of the layer G2 with a metal, and the chemical reaction is followed by removal of non-reacted metal.

22. The method of Claim 17 further comprising, after the operation (g4):

removing the layer L2 to expose an underlying surface of the layer G2; and

reacting the exposed surface of the layer G2 with a conductive material to form a conductive layer on the surface of the layer G2.

23. The method of Claim 22 wherein the conductive layer has a lower resistivity than the layer G2.

24. The method of Claim 22 further comprising, before the reacting operation, forming dielectric on at least portions of sidewalls of the layer G2, wherein the conductive layer is formed selectively on the exposed surface of the layer G2 but not on the dielectric.

25. The method of Claim 22 wherein the reacting operation comprises a reaction with a metal.

26. The method of Claim 22 wherein:

the first conductive gate is part of a first conductive line that provides first conductive gates to a plurality of nonvolatile memory cells;

each of the second conductive gates is part of a second conductive line that provides second conductive gates to said plurality of the memory cells;

the portion P1 and the conductive layer extend along the first conductive line through said plurality of the memory cells, the conductive layer reducing the sheet resistance of the second conductive lines.

27. The method of Claim 22 wherein the memory cell comprises a source/drain region in the semiconductor substrate, and the conductive layer forms on the source/drain region.

28. A method for fabricating an integrated circuit which comprises a nonvolatile memory which comprises an array of nonvolatile memory cells, the integrated circuit comprising an array area containing the array, each memory cell of the array having a first conductive gate and having at least two conductive floating gates FG1 and FG2, the method comprising:

(i) forming one or more conductive lines G1, wherein each first conductive gate comprises a portion of a line G1;

(ii) forming a layer G2 over the first conductive lines, each memory cell having at least two second conductive gates comprising a portion of the layer G2, the layer G2 having a portion P1 protruding above each conductive line G1;

(iii) forming a layer L1 over the layer G2 such that the protruding portions P1 of the layer G2 are exposed and not completely covered by the layer L1;

(iv) partially removing the protruding portions P1 of the layer G2 to form a gap in the layer G2 over each line G1, wherein at a conclusion of this removing operation a portion of the layer G2 remains covered by the layer L1;

(v) forming a layer L2 on the layer G2 adjacent to the gaps; and

(vi) removing at least parts of the layer L1 and the layer G2 selectively to the layer L2.

29. The method of Claim 28 wherein each second conductive gate is a control gate.

30. The method of Claim 28 wherein the operation (iii) comprises:

forming the layer L1 over the entire layer G2; and

planarizing the layer L1 to expose the protruding portions P1.

31. The method of Claim 28 wherein the operation (v) comprises reacting the layer G2 with another material to form the layer L2.

32. The method of Claim 31 wherein the reacting operation comprises oxidation of the layer G2.

33. The method of Claim 31 wherein the reacting operation comprises a chemical reaction of the layer G2 with a metal, and the chemical reaction is followed by removal of non-reacted metal.

34. The method of Claim 28 further comprising, after the operation (vi):

removing the layer L2 to expose an underlying surface of the layer G2; and

reacting the exposed surface of the layer G2 with a conductive material to form a conductive layer on the surface of the layer G2.

35. The method of Claim 34 wherein the conductive layer has a lower resistivity than the layer G2.

36. The method of Claim 34 further comprising, before the reacting operation, forming dielectric on at least portions of sidewalls of the layer G2, wherein the conductive layer is formed selectively on the exposed surface of the layer G2 but not on the dielectric.

37. The method of Claim 34 wherein the reacting operation comprises a reaction with a metal.

38. The method of Claim 34 wherein:

each of the second conductive gates is part of a second conductive line that provides second conductive gates to said plurality of the memory cells;

the portion P1 and the conductive layer extend along the conductive line G1 through said plurality of the memory cells, the conductive layer reducing the sheet resistance of the second conductive lines.

39. The method of Claim 34 wherein the memory cell comprises a source/drain region in the semiconductor substrate, and the conductive layer forms on the source/drain region.

40. A nonvolatile memory cell comprising:

floating gates FG1, FG2; and

a first conductive gate for accessing the floating gates FG1, FG2;

wherein a width of the first conductive gate is smaller than a width of at least one of the floating gates FG1, FG2.

41. The memory cell of Claim 40 wherein the width of the first conductive gate is smaller than the width of any one of the floating gates FG1, FG2.

42. The memory cell of Claim 40 further comprising:

two source/drain regions in a semiconductor substrate; and

a channel region extending between the two source/drain regions in the semiconductor substrate;

wherein the first conductive gate and the floating gates FG1, FG2 overlie the channel region, the first conductive gate being positioned between the floating gates FG1, FG2.

43. An integrated circuit comprising a nonvolatile memory cell, the integrated circuit comprising:

a semiconductor substrate;

a first dielectric region on the semiconductor substrate;

a first conductive gate on the first dielectric region, the first conductive gate being part of the memory cell;

at least two second dielectric regions on the semiconductor substrate;

at least two conductive floating gates on the respective two second dielectric regions, the floating gates being part of the memory cell, the two floating gates being adjacent to respective two sidewalls of the first conductive gate;

a dielectric layer comprising at least two continuous features, each feature overlying a respective one of the floating gates and also overlaying a respective one of the sidewalls of the first conductive gate;

at least two second conductive gates, each second conductive gate overlying a respective one of the floating gates and a respective one of the continuous features of the dielectric layer, the respective continuous feature of the dielectric layer also separating the second conductive gate from the first conductive gate, the second conductive gates being part of the memory cell.

44. The integrated circuit of Claim 43 wherein the memory cell further comprises two source/drain regions of a first conductivity type in the semiconductor substrate, and a channel region of a second conductivity type in the semiconductor substrate, the channel region extending under the first conductive gate and the two floating gates between the two source drain regions.

45. The integrated circuit of Claim 43 wherein the dielectric layer comprises a silicon nitride layer.

46. The integrated circuit of Claim 43 wherein the dielectric layer comprises ONO.

47. The integrated circuit of Claim 43 wherein the memory cell is one of a plurality of memory cells;

wherein the semiconductor substrate comprises a plurality of substrate isolation regions between active areas of the semiconductor substrate, each substrate isolation region being a dielectric region protruding above the semiconductor substrate;

wherein each memory cell comprises a first dielectric region on an active area of the semiconductor substrate;

wherein the first conductive gate is part of a conductive line G1 which crosses over a plurality of the substrate isolation regions and over the first dielectric regions and provides a first conductive gate to each of the memory cells;

wherein each memory cell comprises two second dielectric regions on the semiconductor substrate, and a conductive floating gate on each of the two second dielectric regions;

wherein each said continuous feature of the dielectric layer overlies one of the floating gates of the memory cells;

wherein the integrated circuit comprises two conductive lines G2, each line G2 providing one of the second conductive gates to each of the memory cells, wherein each line G2 crosses over a plurality of the substrate isolation regions and overlies one of the floating gates of each memory cell, wherein each continuous feature of the dielectric layer is present between a respective one of the floating gates of each memory cell and a respective one of the lines G2, the lines G2 being insulated from the line G1.

48. The integrated circuit of Claim 47 wherein the plurality of memory cells is a row of memory cells in a memory array having a plurality of rows of nonvolatile memory cells;

wherein each memory cell comprises a first dielectric region on an active area of the semiconductor substrate;

wherein the line G1 is one of a plurality of conductive lines G1 each of which crosses over a plurality of the substrate isolation regions and over the first dielectric regions of at least one row of the memory cells and provides a first conductive gate to each memory cell in at least one row of the memory cells;

wherein each memory cell comprises at least two second dielectric regions on the semiconductor substrate, and at least two conductive floating gates on the respective second dielectric regions;

wherein the continuous feature of the dielectric layer is one of a plurality of continuous features of the dielectric layer, wherein each continuous feature overlies the one of the floating gates of each memory cell in at least one row of the memory cells;

wherein the conductive lines G2 are two of a plurality of conductive lines G2, each line G2 providing one second conductive gate to each memory cell in at least one row of the memory cells, wherein each line G2 crosses over a plurality of the substrate isolation regions and overlies one of the floating gates of each memory cell in at least one row of the memory cells, wherein for each line G2 a corresponding continuous feature of the dielectric layer is present between the line G2 and the floating gates overlain by the line G2, the line G2 being insulated from the corresponding line G1.

49. An integrated circuit comprising a nonvolatile memory comprising:

a semiconductor substrate;

a plurality of substrate isolation regions in the semiconductor substrate between active areas of the semiconductor substrate, each substrate isolation region being a dielectric region protruding above the semiconductor substrate;

a plurality of conductive lines G1, each conductive line G1 overlying at least one active area, wherein the nonvolatile memory comprises a plurality of nonvolatile memory cells, each memory cell comprising a first conductive gate comprising a portion of a line G1, each line G1 being insulated from the semiconductor substrate, wherein the top surface of the line G1 is planar but the bottom surface of the line G1 goes up and down over the substrate isolation regions;

a dielectric over two opposite sidewalls of each line G1;

at each of said sidewalls of the lines G1, a plurality of conductive floating gates abutting the dielectric over the respective sidewall of the line G1, the floating gates being insulated from the lines G1 and the semiconductor substrate, each floating gate extending between adjacent substrate isolation regions;

at each of said sidewalls of the lines G1, a conductive line G2 overlying the respective floating gates, each line G2 being insulated from the corresponding line G1 and from the underlying floating gates, each memory cell comprising two of the floating gates and two second conductive gates provided by respective two conductive lines G2.

50. The integrated circuit of Claim 49 wherein the memory comprises an array area comprising an array of said memory cells, and each substrate isolation region traverses the entire array area.